AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for performing a timing analysis for a core device to be embedded in a programmable logic device, comprising:

obtaining clock-to-output timing information for the core device;

determining setup and hold timing information and delay timing information for a portion of the programmable logic device;

associating the clock-to-output timing information, the setup and hold timing information and the delay timing information with respective signals; and

calculating a path time delay for each of the respective signals.

2. (Original) The method of Claim 1 further comprising determining whether the path time delay for each of the respective signals is less than a clock period.

3. (Currently Amended) The method of Claim 2 further comprising modifying the portion of the ~~host integrated circuit~~ programmable logic device in response to the path time delay for at least one of the respective signals being more than the clock period.

4. (Previously Presented) The method of Claim 3 further comprising determining circuitry values in response to modification of the portion of the programmable logic device.

5. (Currently Amended) The method of Claim 3 further comprising feeding back the circuitry values and modifications of the portion of the[[_]] programmable logic device for re-determination of at least one of the setup and hold timing information and the delay timing information for the portion of the programmable logic device.

6. (Previously Presented) The method of Claim 5 wherein the portion of the programmable logic device comprises logic and interconnects for coupling the core device to the programmable logic device.

7. (Previously Presented) The method of Claim 6 wherein the portion of the programmable logic device comprises a memory controller coupled to the logic and interconnects.

8. (Currently Amended) The method of Claim 7 wherein the core device is a microprocessor[[,]] .

9. (Original) The method of Claim 8 wherein the programmable logic device is a field programmable gate array.

10. (Currently Amended) A method for performing a timing analysis for a core device in a host integrated circuit, comprising:

obtaining setup and hold timing information for the core device;

determining clock-to-output timing information and delay timing information for a portion of the host integrated circuit;

associating the clock-to-output timing information, the setup and hold timing information and the delay timing information with respective signals;

calculating a path time delay for each of the respective signals;

modifying the portion of the host integrated circuit [[is]] in response to the path time delay for at least one of the respective signals being more than the clock period;

determining circuitry values in response to modification of the portion of the host integrated circuit; and

feeding back circuitry values and modifications of the portion of the host integrated circuit for re-determination of at least one of the clock-to-output timing information and the delay timing information for the portion of the host integrated circuit.

11. (Original) The method of Claim 10 further comprising determining whether the path time delay for each of the respective signals is less than a clock period.

Claims 12-14. (Cancelled)

15. (Currently Amended) The method of Claim [[12]]10 wherein the portion of the host integrated circuit comprises logic and interconnects for coupling the core device to the host integrated circuit.

16. (Original) The method of Claim 15 wherein the portion of the host integrated circuit comprises a memory controller coupled to the logic and interconnects.

17. (Original) The method of Claim 16 wherein the core device is a microprocessor, and wherein the host integrated circuit is a programmable logic device.

18. (Original) The method of Claim 17 wherein the programmable logic device is a field programmable gate array.

Claims 19-34 (Cancelled)